E1-32XSR

RISC/DSP Processor

E1

hyperstone®


hyperstone
E1-32XSR
0405FK1HH
S27124.1
ETHERNET
IEEE
1588
HYNETOS

E1-32XSR

RISC/DSP Processor

A 32-Bit microcontroller design with an integrated RISC/DSP core architecture offering maximum power-efficiency for portable multimedia and consumer electronics applications.

RISC and DSP Working Together

The new E1-32XSR offers a powerful RISC architecture with integrated DSP support and 16KByte on-chip SRAM. This unique integrated design delivers a power-efficient and cost-effective solution for a wide range of portable multimedia and consumer electronic products. Now developers can have the best of both worlds – a fast RISC processor for control functions, and a DSP unit for efficient algorithm execution – yet avoid the silicon overhead and software complexity of a dual-core design.

General Architecture

The E1-32XSR is based on a load/store architecture built around a large register set that includes 64 general-purpose and 32 special-purpose registers, as well as an instruction buffer of 128 bytes. Local registers are organized into a 64-word, circular register stack to hold function/subroutine stack frames. The stack is organized into frames comprising up to 16 words; the E1-32XSR keeps current frames on-chip and automatically pushes the frame to memory as the register stack fills and moves frames back as the register stack empties. For fast parameter passing, the current stack frame can overlap the previous one with a variable range. Other on-chip resources include 16KByte of single-cycle access fully static SRAM, a memory and peripheral-interface controller and 3 programmable I/O lines. An integrated PLL is user programmable and allows for multiplication of the external clock by a factor of 0.5/1/2/4 and 8.

The variable-length 16, 32, or 48-Bit instructions, automatically pre-fetched by the E1-32XSR, support constants and native addresses of 16 and 32-Bits. A 2-stage pipeline accelerates standard or delayed branches. The 4-GByte address memory space is divided into seven blocks: internal functions, on-chip SRAM and 5 external memory areas; each external block can be user-configured in software for bus width, timing and memory type. The memory interface supports glueless connection of DRAM, SRAM, EPROM, FlashEPROM or other memory mapped devices. The separate I/O-address space also allows each I/O device to have its own timing.

Key Data

- Integrated RISC/DSP core with peak performance
- Single RISC/DSP instruction stream for rapid development and simplified debugging environment
- Parallel execution of Load/Store, RISC and DSP Units
- Very high code density using variable length 16, 32 and 48-Bit instructions
- Extremely low interrupt latency - starts code execution in less than 50 ns
- Low power consumption of 200 mW at 2.5 V using 0.25 µm technology
- Power-efficient performance of integrated core delivers peak throughput of 3.6 GOPS/Watt
- Available in 16 or 32-Bit external bus interface versions, both with full internal 32-Bit execution
- Available as “off-the-shelf” standard LQFP devices or as IP core for ASIC integration

Power Supply Voltage

The E1-32XSR is designed for a core voltage of 2.5V. Interface to external memory and I/O can be 2.5V or 3.3V.

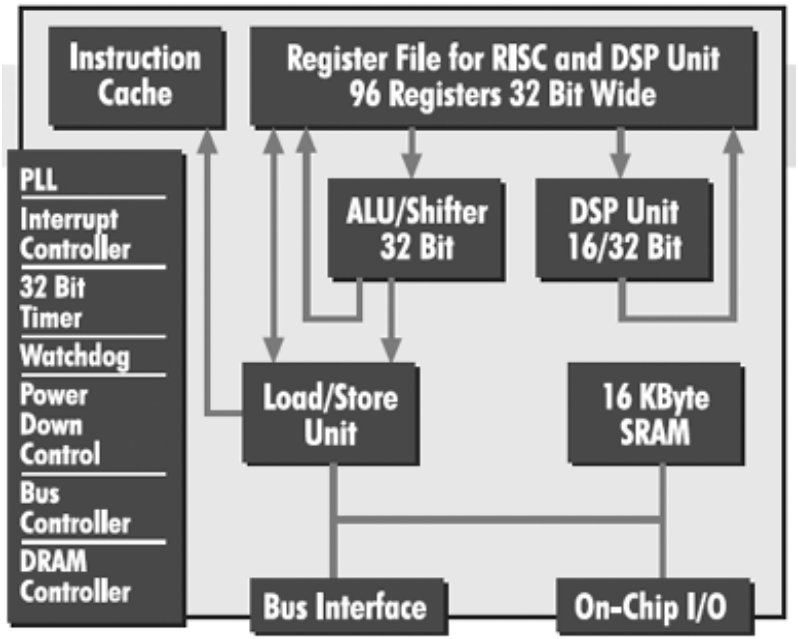
Environmental Rating

Temperature range is 0 to 70°C for the commercial and –40 to +85°C for the industrial product range.

E1-32XSR

RISC/DSP Processor

E1-32XSR Block Diagram



Quality and Environmental Matters

Starting immediately, customers can order Pb-free products in line with the requirements of the Waste Electrical and Electronic Equipment (WEEE) and Restriction of Hazardous Substances (RoHS) directives. Please ask specifically for Pb-free parts if you require für Pb-free compatible manufacturing capability.

E1-32XSR

RISC/DSP Processor

Integrated Core Functionality

The Hyperstone core has been specifically designed to combine both RISC and DSP functions – but as a single integrated core and instruction set, rather than a combination of two different cores on a single piece of silicon. This fully integrated core is based on a single processor model with a single instruction stream. Simple and efficient communication between the RISC and DSP units is achieved via the 96-way 32-Bit internal register set. A major factor in achieving the high power-efficiency of this design is the parallel operation of three functional blocks of the integrated core: the RISC ALU, the DSP Unit and the Load/Store Unit. The integrated architecture allows instructions to be streamed through all 3 units simultaneously to deliver a peak performance of 380 MOPS.

DSP Capabilities

The fully integrated DSP unit, working in parallel with the ALU and the load/store unit, can perform DSP calculations while the ALU is performing loop counts, address calculations, or load-and-store operations. The DSP unit shares all of the functional blocks of the E1-32XSR, including the register set; however, it uses dedicated result registers and 32 and 64-Bit hardware accumulators. The DSP unit supports 16 and 32-Bit fixed-point or integer data types. The special DSP instructions include 16x16 and 32x32 multiply, complex and real multiply-accumulate, multiply-subtract, and complex addition/subtraction. Other special instructions include test-leading-zeros.

DRAM Support

The E1-32XSR incorporates a DRAM controller on-chip that allows the user to program page size, refresh rate, timing, and access parameters by using on-chip registers. The controller supports SDRAMs as well as fast-page-mode and extended-data-out DRAMs. Each of five external memory blocks can be supported with independent timing and bus width.

Interrupt Latency

The E1-32XSR is designed for very fast interrupt response. An interrupt service routine will commence within 7 clock cycles, unless blocked by a higher priority interrupt. This results in the start of code execution in less than 50 ns, at a clock rate of 180MHz. In addition to the internal interrupts, 7 external priority-controlled interrupts are provided.

Timer Support

The on-chip hardware timer is coupled to the clock via a programmable pre-divider (factors from 2 to 257). Running at speeds up to 90 MHz, this provides a resolution of about 10 ns for interrupt generation. Using the hyRTK kernel, the user has access to 254 independent “virtual“ timers with very low processing overhead.

Power Management Support

Ultra low system power consumption can be achieved by using the various on-chip mechanisms of this fully static design. In Power-Down Mode, only the interrupt logic, clock, timer, and DRAM-refresh logic remain active. Sleep Mode additionally disables external DRAM refresh. At 2.5V, current consumption in power-down and sleepmodes is less than 2 mA and 100 µA, respectively. The integrated PLL function is software programmable and provides opportunities for additional power management by modifying the internal clock frequency with multiplication factors of 1/2, 1, 2, 4 and 8, dynamically programmable according to application requirements.

Packaging

The E1-32XSR is available in a 144 pin LQFP, and the E1-16XSR as a 100 pin LQFP.

hyperstone®

Hyperstone GmbH
Line-Eid-Strasse 3
78467 Konstanz
Germany
Phone: +49 7531 98030
Fax: +49 7531 51725
Email: info@hyperstone.de
www.hyperstone.com

Hyperstone Inc. - USA
4800 Bethania Station Road
Winston-Salem, NC 27105
USA
Phone: +1 336 744 0724
Fax: +1 336 744 5054
Email: us.sales@hyperstone.com

Hyperstone Asia Pacific - Taiwan
3F, No. 501, Sec.2, TidingBlvd.
Neihu District, Taipei City 114
Taiwan, R.O.C.
Phone: +886 2 8751 0203
Fax: +886 2 8797 2321
Email: taiwan@hyperstone.com

HS-Mkt_E1_AS-07-08-21