E2 RISC/DSP Microcontroller

E2

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RISC/DSP

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RISC/DSP Microcontroller

The Hyperstone E2 microcontroller combines a high-performance RISC processor with a powerful DSP unit. Additional on-chip highlights include a programmable serial communication engine, an analog to digital converter (ADC), and a full 32 kBytes of on chip (I-RAM) complemented by a flexible external memory and peripheral interface controller. Maximum efficiency in terms of power consumption, gate count, and ease of programming, when utilizing RISC and DSP functionality, are inherent features of the unique Hyperstone RISC/DSP architecture.

- **32-Bit unified RISC & DSP processor architecture**
- **Peak performance of 640 MOPS and 160 MHz**
- **Dynamic frequency scaling, power down and sleep mode**
- **Power consumption of about 200 mW typical**
- **Instruction set compatible to all Hyperstone E1 based controllers**
- **Parallel execution of ALU, DSP, and load/store instructions**
- **Very high code density using variable length 16, 32, and 48-Bit instructions**
- **32 kByte fully static on-chip memory (I-RAM)**
- **Programmable 8-channel serial communication engine**
- **Implementation of 4 UART ports possible**
- **10-Bit, 8-channel multiplexed A/D-converter with sample rate of 182 kHz**
- **Versatile 2-channel DMA engine for I/O device data transfer**
- **Battery backed real time clock**

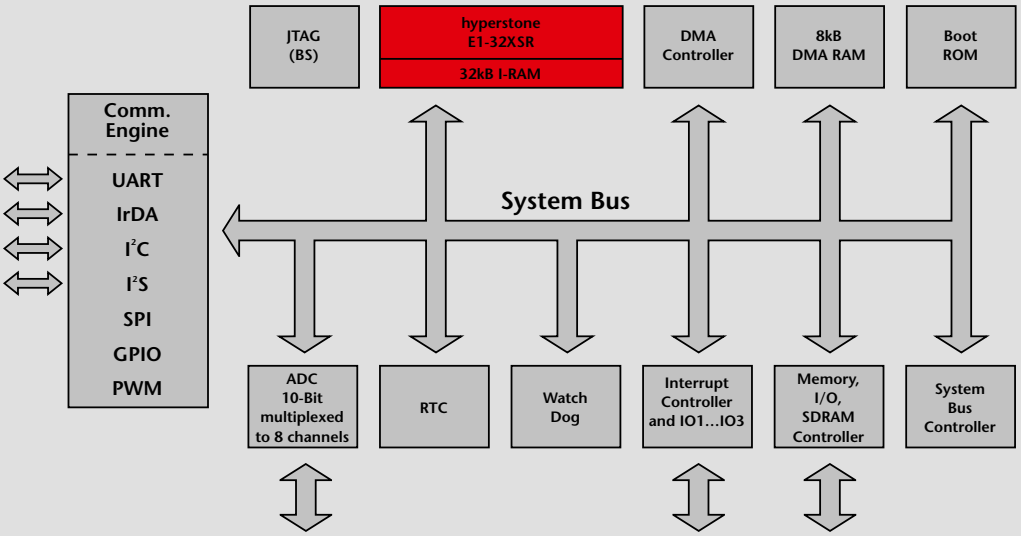
Development Tools

- Development kit including board, serial debug interface
- Integrated Development Environment (IDE), C/C++ compiler, linker, assembler, source-level debugger with profiler, runtime kernel, and DSP library

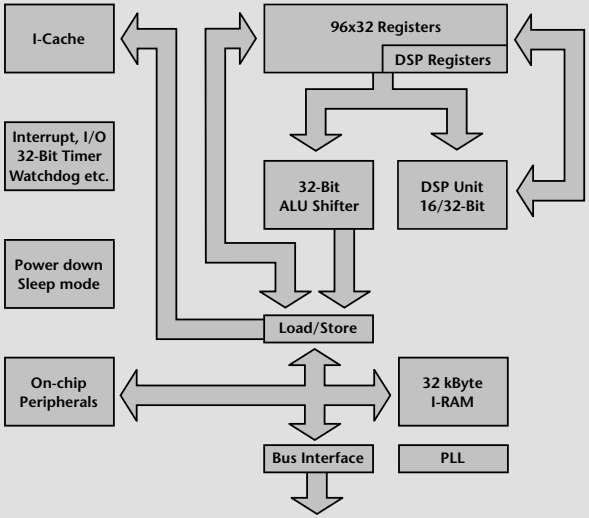
Order Information

- E2-LBL07---144 pin LQFP, RoHS, 0 to +70 °C
- E2-RBL07---144 pin LQFP, RoHS, -40 to +85 °C
- EV13-E2-LBL07: Development Board

Block Diagram E2 – RISC/DSP Microcontroller



Block Diagram E1-32XSR – RISC/DSP Processor Core Architecture



RISC/DSP Processor Core Architecture & Instructions

- Load/store architecture
- 96 registers organized into 64 general-purpose and 32 special-purpose registers, 32-Bits each
- 32 global and 64 local registers of which 16 global and up to 16 local registers can be addressed directly
- Instruction buffer of 128 Bytes
- Local registers organized in 64-word, circular register stack holding function/subroutine stack frames
- Stack organized in frames comprising up to 16 words
- Frames are automatically moved between memory and register stack, for fast parameter passing, the current stack frame can overlap the previous one with variable range
- Fast Call and Return by parameter passing via registers
- Pipelined memory access
- 2 stage pipeline – decode/execute – branching without wait cycles for delayed branch instructions
- Variable 16, 32, and 48-Bit instructions length
- Parallel execution of ALU, DSP, and load/store instructions
- Most instructions execute within one cycle
- Pipelined DSP instructions
- Single-cycle half-word multiply-accumulate operation
- Range and pointer checks are performed without any performance penalty

Serial Communication Engine & Analog to Digital Converter

- 16 GPIOs assigned to eight channels
- I2C support for a two-wire multi-master interconnect master and slave mode
- UART support for up to 4 ports
- 10-Bit multiplexed to 8 channels with sample rate of 181.6 kHz

Memory and I/O Controller and Bus Interface

- Memory and peripheral-interface controller where bus width, timing and memory type for 5 external memory areas can be user-configured supporting glue-less connection of DRAM, SRAM, EPROM, Flash or other memory mapped devices.
- 3 separate programmable I/O lines and address space allows each I/O device to have its own timing
- Separate address bus of 22-Bits and data bus of 16-Bits provide a throughput of up to two bytes at each clock cycle
- Data bus width of 16 or 8 Bits, individually selectable for each external memory area
- Flexible boot options including 8-Bit and 16-Bit NOR flash, NAND flash, SPI flash, and I2C flash
- In-system flash programming through SIO boot loader
- Configurable I/O pins
- Internal generation of all memory and I/O control signals
- Wait pin function for I/O accesses to peripheral devices, and for memory accesses to MEM2
- On-chip DRAM controller supporting Fast-Page-Mode DRAMs, EDO DRAMs, and synchronous DRAMs (SDRAM)
- Control function for CLKOUT pin
- Versatile 2-channel DMA controller for I/O device data transfer

Timers & Power Management

- Two separate multi-functional timers
- Phased locked loop (PLL) settings controllable by software provide clock rate multipliers of ½, 1, 2, 4, or 8
- Power-down Mode and Sleep Mode
- Battery backed real time clock

Internal Memories

- 32 kByte of single-cycle access fully static SRAM (I-RAM)
- 8 kByte of single-cycle access fully static SRAM for DMA
- 8 kByte boot ROM

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