hyNet® S

Communication Controller

hyperstone®


Serial (UART, SPI, I²C, I²S, IrDA)
DCT
Ethernet
PCI
CAN
YUV
hyperstone
hyNet S
0405FK1HH
S27124.1
EtherNet/IP
ETHERNET POWERLINK
IEEE 1588
HYNETOS

hyNet® S

Communication Controller

Benefit from both: the unique, highly efficient and easy to program Hyperstone RISC/DSP architecture combined with the most necessary interfaces and features required for network enabling and communications within the embedded applications world. Furthermore, integrating features such as an automatic JPEG encoder and CMOS sensor interface, hyNet® S offers a single chip IP-camera.

- **Highly integrated System on Chip helps to reduce application costs**
- **Excellent RISC/DSP performance of up to 180 MIPS and 720 MOPS**
- **Versatile interface options**
- **Power-saving features and efficient realization guarantee highly energy-efficient chip**
- **Easy programming of RISC and DSP**

Targeted Applications

- Security Applications
- Internet Protocol Cameras (IP-Cam)
- Digital Video Recorders (DVR)
- Data and Voice over IP (VoIP)
- Cost sensitive network-enabling and embedded web servers
- Industrial Automation, Control and Robotics
- Real-Time Ethernet, PROFINET, Ethernet Powerlink, Ethernet/IP
- Bus Bridges (e.g. Serial to Ethernet)

  ...and many more

High Performance Hyperstone Processor Architecture

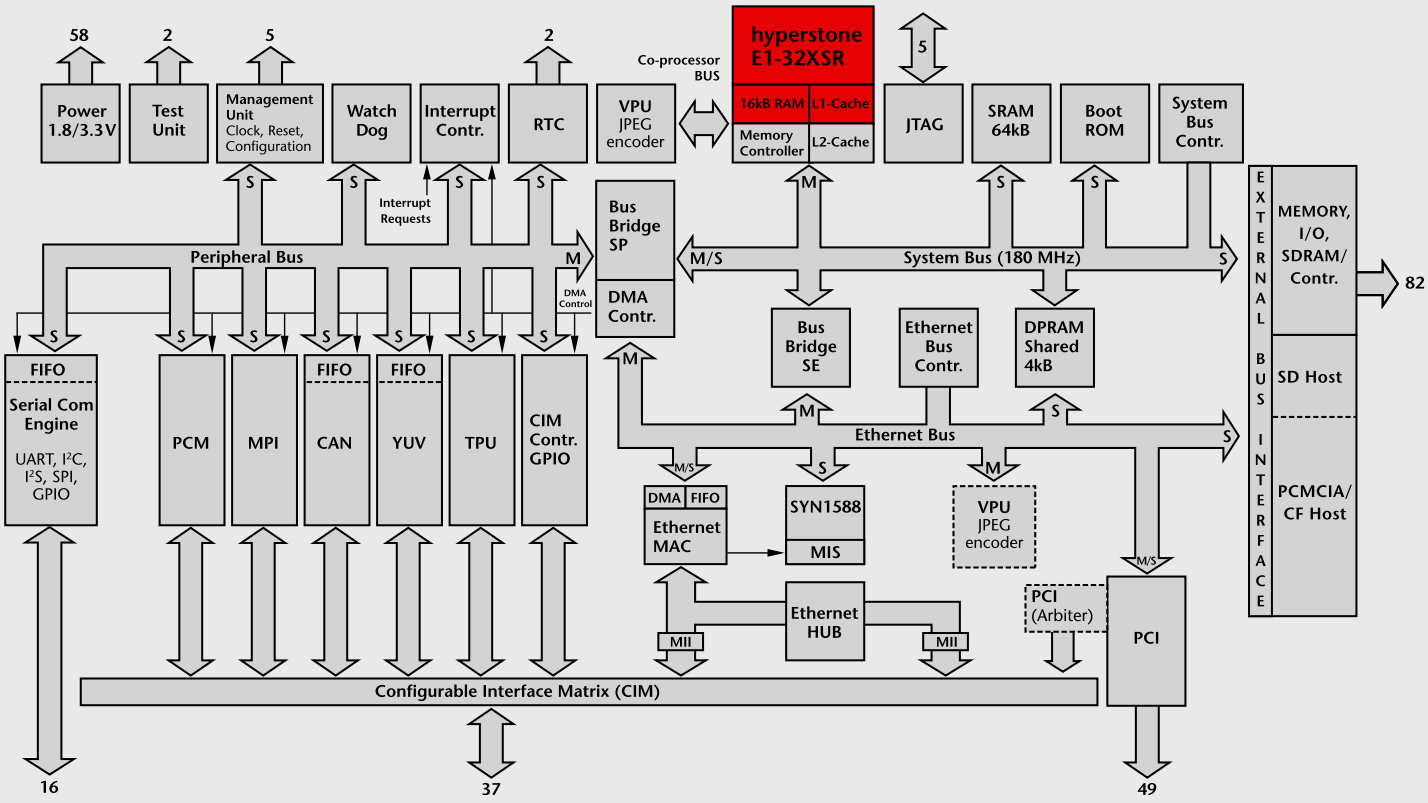
- Hyperstone 32-Bit RISC/DSP processor core (E1-32XSR)
- Up to 180 MHz, dynamic frequency scaling delivering 180 MIPS and up to 720 MOPS
- Latency based parallelism of RISC ALU, Load/Store and DSP
- Comprehensive DSP Library

  ...and many more

Key Data

- 256 pin TFBGA package, RoHS compliant;
  17 x 17 x 1.4 mm, 1.0mm ball pitch
- Core-Voltage: 1.8 V, I/O Voltage: 3.3V
- Industrial Temperature Range: -40 to 85°C
- Manufactured in 0.18 µm process
- Maximum power consumption worst case: < 800 mW

hyNet® S Block Diagram



Development Hardware and Software Support

All development hard- and software is available from Hyperstone and partners for Windows® and Linux based host systems. An inexpensive starter-kit includes evaluation board, ECLIPSE open-source Integrated Development Environment (IDE), C/C++ compiler (based on GNU Compiler Collection – GCC), GNU linker, assembler, libraries including DSP library and library manager, GNU Source-Level Debugger, and GNU application debugger for µCLinux.

Key Features

- 4 internal busses with multi channel DMA controller
  - Peripheral Bus with variable frequency, to reduce power consumption
  - Multi-master/multi-slave high frequency System Bus
  - Ethernet Bus
  - Co-processor Bus
- External Bus Interface with variable timing and bus widths of 8, 16 or 32-Bit
- Direct Memory Access Controller with 3 independent configurable channels
- Efficient Power Management
- Management Unit including reset manager, clock manager and configuration unit
- Interrupt Controller
- Time Processor Unit (TPU) programmable timer with one 32-Bit counter and two 16 Bit counters e.g. for pulse width modulation (PWM)
- Video Processing Unit (VPU): automatic JPEG encoding, providing 4.2.2, 4.2.0 and 4.0.0 output formats
- JTAG (Boundary Scan) compliant to the IEEE P1149.1
- Real Time Clock
- Watchdog

Internal Memory-System

- CPU core: 16 kByte RAM, two 2 kByte instruction / data caches (L1)
- 8 kByte Mask ROM (Boot loader)
- 64 kByte SRAM
- 4 kByte shared DPR (Ethernet)
- 32-Bit data and address bus

Versatile Interfaces

- 10/100 Mbit/s Ethernet MAC with two MII including ultra-fast 3-port Ethernet Hub (2 external and 1 internal MII); fully compliant with Ethernet standards such as IEEE 802.3, 802.3u, and ANSI X3.263-1995 (FDDI-TP- PMD)
- IEEE 1588 Clock Synchronization Unit
- 32-Bit PCI interface, 33 or 66 MHz, host and limited target mode (3.3V supply only), compliant to PCI 2.2, Mini PCI 1.0
- YUV interface CCIR656 / 601-compliant video interface 8-Bit
- PCM Interface connecting to an external IOM-2 bus (ISDN)
- Controller Area Network (CAN) interface compatible to CAN 2.0, extended format and Philips SJA1000; featuring non-destructive bit-wise arbitration (CSMA / CA), message based addressing / filtering, broadcast communication, and 1Mbit / sec operation
- Multiplexed Processor Interface (MPI) to connect co-processors e.g. for powerline communication
- Programmable Serial Communication Engine, 16 I/O lines or software controlled general purpose I/Os, providing eight communication channels including UART, IrDA, SPI, I^2S, I^2C Master and Slave, synchronous communication and interface options to various devices such as A/D or D/A converters, codecs and serial memories

hyperstone®

Hyperstone AG
Line-Eid-Strasse 3
78467 Konstanz
Germany
Phone: +49 7531 98030
Fax: +49 7531 51725
Email: info@hyperstone.de

Hyperstone Inc. - USA
4800 Bethania Station Road
Winston-Salem, NC 27105
USA
Phone: +1 336 744 0724
Fax: +1 336 744 5054
Email: us.sales@hyperstone.com

Hyperstone Asia Pacific - Taiwan
11F, No. 183, Sec.2, TidingBlvd.
Neihu District, Taipei City 114
Taiwan, R.O.C.
Phone: +886 2 8751 0203
Fax: +886 2 8797 2321
Email: taiwan@hyperstone.com

www.hyperstone.com

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