hyNet® XS

Communication Controller

XS

hyperstone®


Serial
Ethernet
(MAC+PHY)
USB
CAN
hyperstone
hyNet XS
0405FK1HH
S27124 .1
PROFINET
EtherNet/IP
ETHERNET POWERLINK
IEEE 1588
HYNETOS

hyNet® XS

Network Communication Controller

Benefit from both, the unique, highly efficient and easy to program Hyperstone RISC/DSP architecture combined with the most necessary interfaces and features required for network enabling and communications within the embedded applications world. Together with available software solutions and a boot via the network option, hyNet® XS comprises a true system on a single chip.

- **Highly integrated System on Chip including integrated PHY helps to reduce application costs**
- **Excellent RISC/DSP performance of up to 200 MIPS and 800 MOPS**
- **Versatile interface options**
- **Power-saving features and efficient realization guarantee highly energy-efficient systems**
- **Easy programming of RISC and DSP**

Targeted Applications

- Industrial Automation, Control and Robotics
- Real-Time Ethernet, PROFINET, Ethernet Powerlink, Ethernet/IP
- Cost sensitive network-enabling and embedded web servers
- Communication infrastructure
- Bus Bridges
- Data and Voice over IP (VoIP)
- Residential Gateways
- Power line communications

  ... and many more

High Performance Hyperstone Processor Architecture

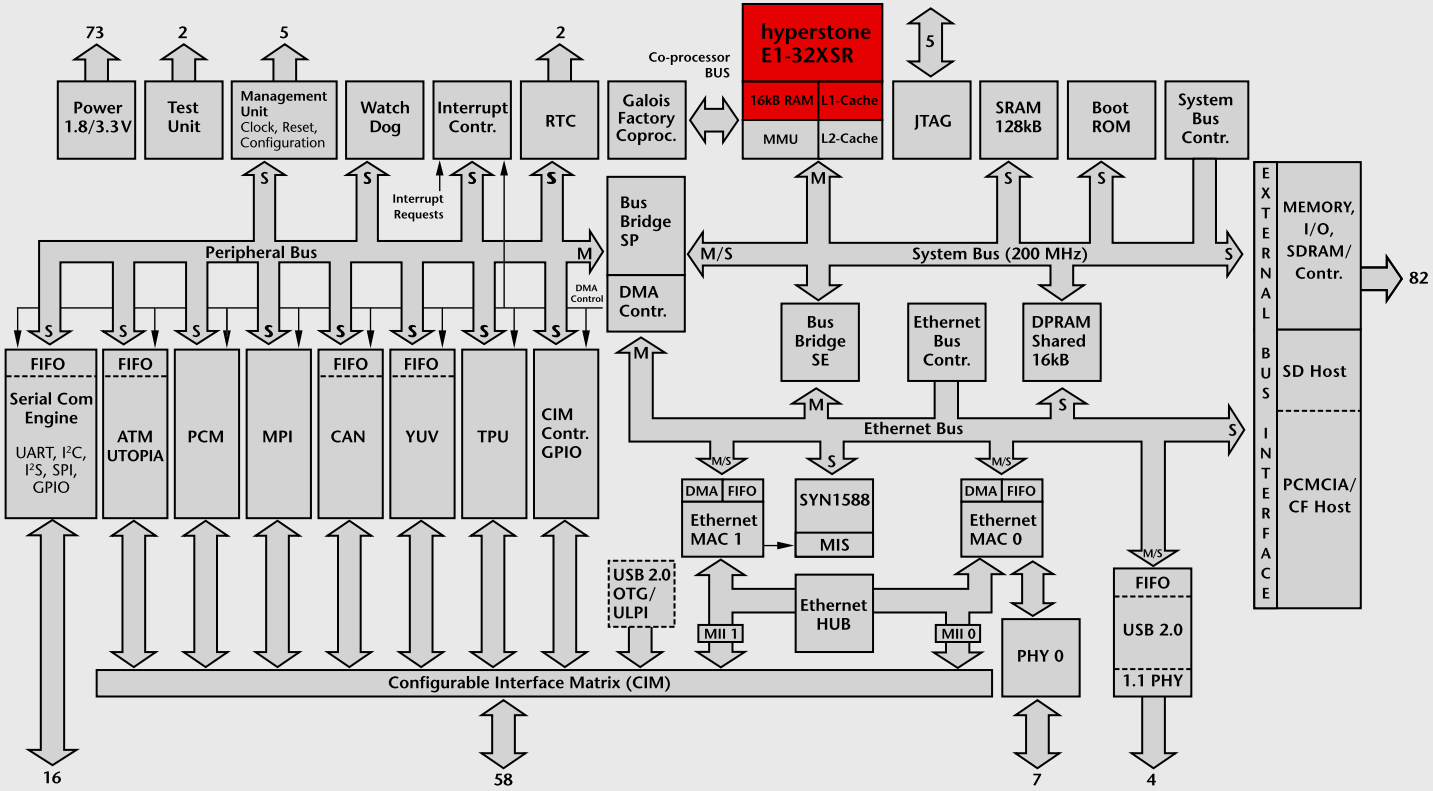
- Hyperstone 32-Bit RISC/DSP processor core (E1-32XSR)
- Up to 200MHz, dynamic frequency scaling delivering 200 MIPS and up to 800 MOPS
- Latency based parallelism of RISC ALU, Load/Store and DSP
- Comprehensive DSP Library

  ... and many more

Key Data

- 256 pin TFBGA package, RoHS compliant; 17 x 17 x 1.4 mm, 1.0mm ball pitch
- Core-Voltage: 1.8V, I/O Voltage: 3.3V
- Industrial Temperature Range: -40 to 85°C
- Manufactured in 0.18µm process
- Maximum power consumption worst case: <1.5 Watts

hyNet® XS Block Diagram



Development Hardware and Software Support

All development hard- and software is available from Hyperstone and partners for Windows® and Linux based host systems. An inexpensive starter-kit includes evaluation board, ECLIPSE open-source Integrated Development Environment (IDE), C/C++ compiler (based on GNU Compiler Collection - GCC), GNU linker, assembler, libraries including DSP library and library manager, GNU Source-Level Debugger, and GNU application debugger for Linux.

Key Features

- 4 internal busses with multi channel DMA controller
  - Peripheral Bus with variable frequency, to reduce power consumption
  - Multi-master/multi-slave high frequency System Bus
  - Ethernet Bus
  - Co-processor Bus
- External Bus Interface with variable timing and bus widths of 8, 16 or 32-Bit
- Direct Memory Access Controller with 6 independent configurable channels
- Memory Management Unit (MMU)
- Efficient Power Management
- Management Unit including reset manager, clock manager, configuration unit
- Interrupt Controller
- Time Processor Unit (TPU) programmable timer with one 32-Bit counter and two 16-Bit counters e.g. for pulse width modulation (PWM)
- Galois Factory Coprocessor: hardware calculation of Galois field operations, Reed-Solomon error correction codes
- JTAG (Boundary Scan) compliant to the IEEE P1149.1
- Real Time Clock, battery buffered
- Watchdog

Internal Memory-System

- CPU core: 16 kByte RAM, two 2 kByte instruction / data caches (L1)
- 8 kByte Mask ROM (Boot loader)
- 128 kByte SRAM
- 16 kByte shared DPR (Ethernet)
- 32-Bit data and address bus

Versatile Interfaces

- Dual 10/100 Mbit/s Ethernet MAC with two MII including ultra-fast 3-port Ethernet Hub (2 external and 1 internal MII) and one Ethernet PHY; fully compliant with Ethernet standards such as IEEE 802.3, 802.3u, and ANSI X3.263-1995 (FDDI-TP- PMD)
- IEEE 1588 Clock Synchronization Unit
- USB 2.0 on-the-go (OTG) controller with integrated USB 1.1 transceiver (supporting up to 12Mbit/s serial data transmission), optionally ULPI interface for external USB 2.0 PHY to increase speed and/or little external logic to enable OTG functionality
- YUV interface CCIR656 / 601-compliant video interface 8/16-Bit
- PCM Interface connecting to an external IOM-2 bus (ISDN)
- Controller Area Network (CAN) interface compatible to CAN 2.0, extended format and Philips SJA1000; featuring non-destructive bit-wise arbitration (CSMA / CA), message based addressing / filtering, broadcast communication, and 1Mbit / sec operation
- Asynchronous Transfer Mode (ATM) – UTOPIA Level-2 Interface, for connection of up to 3 external ATM physical layer controller (DSL)
- Multiplexed Processor Interface (MPI) configurable for CPU independent external transfers, accessible directly by the CPU or DMA, connects up to 15 external Power Line physical layer controllers for TDM transmission
- Programmable Serial Communication Engine, 16 I/O lines or software controlled general purpose I/Os, providing eight communication channels including UART, IrDA, SPI, I^2S, I^2C Master and Slave, synchronous communication and interface options to various devices such as A/D or D/A converters, codecs and serial memories.

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HS-Mkt-AM-06-08-01